

# "Solar Energy" WS 2021/2022

#### **PV Technology:**

#### Lecture 7: Crystalline Silicon (c-Si) Solar Cells

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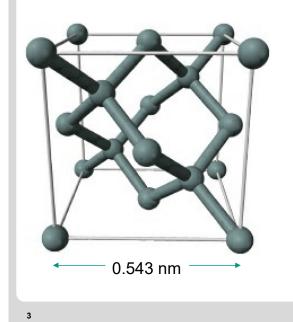
KIT - the Research University of the Helmholtz Association

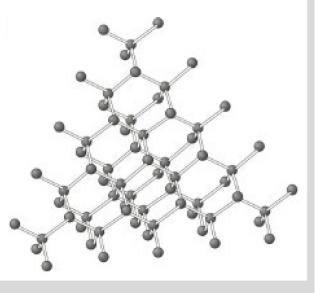
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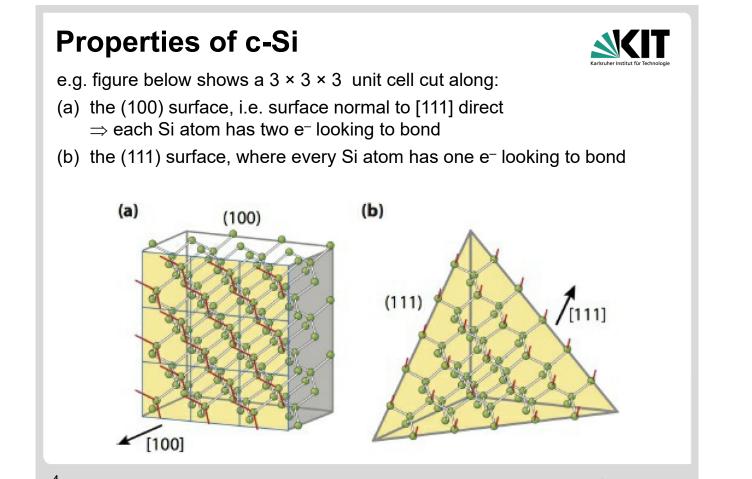
Crystal lattice is not the same in every direction

e.g. if we make large cuts through the lattice, the various planes would not look the same





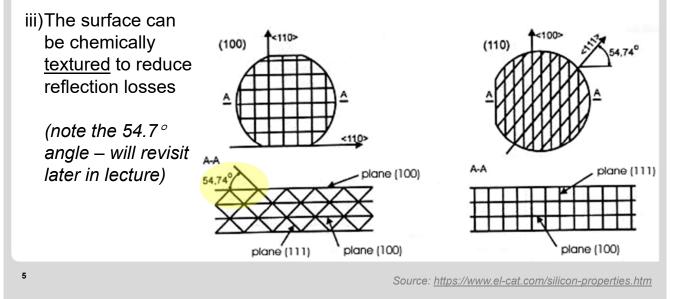
Source: textbook





(100) c-Si wafers normally used making solar cells – three advantages:

- i) Lowest density of surface atoms (6.8×10<sup>14</sup>/cm<sup>2</sup>) compared to other planes
- ii) Interface between (100) Si and SiO<sub>2</sub> demonstrated to have lowest <u>defect</u> <u>density</u>  $\Rightarrow$  less recombination  $\Rightarrow$  lower  $J_0 \Rightarrow$  higher  $V_{oc}$



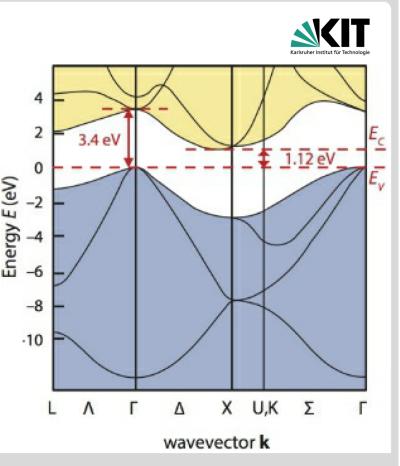
#### **Properties of c-Si**

c-Si has bandgap energy  $E_g \sim 1.12 \text{eV} (\lambda \sim 1100 \text{ nm})$ 

This bandgap is <u>indirect</u> is  $\Rightarrow$  i.e. energy as well as momentum required to excite charge carriers from valence band to conduction band

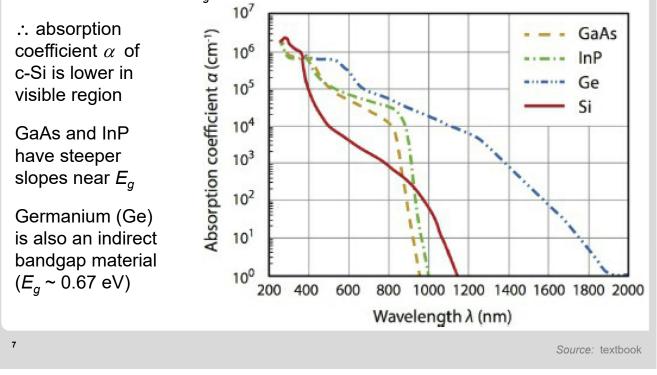
c-Si has direct transitions too, but these are in UV, e.g  $E_{g\text{-direct}} = 3.4 \text{ eV}$ ( $\lambda = 364 \text{ nm}$ )

Additional momentum given to charge carriers via <u>phonons</u> (lattice vibrations)



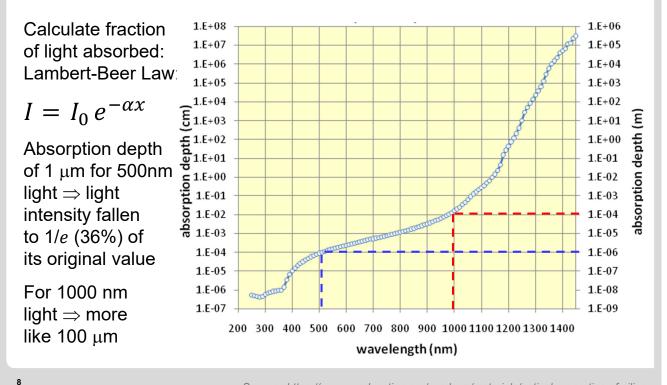


Due to required change in momentum  $\Rightarrow$  indirect bandgap material less likely to absorb photon with energy >  $E_g \Rightarrow$  e.g. compared to direct bandgap materials with similar  $E_q$ , gallium arsenide (GaAs), indium phosphide (InP)



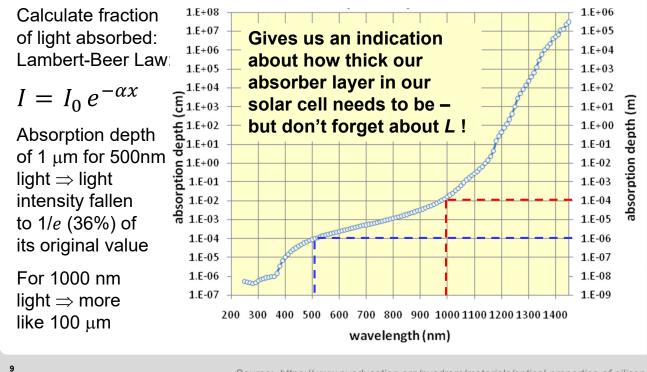
#### **Properties of c-Si**

Can also consider the absorption depth  $\alpha^{-1}$  (a.k.a. penetration depth)





Can also consider the absorption depth  $\alpha^{-1}$  (a.k.a. penetration depth)

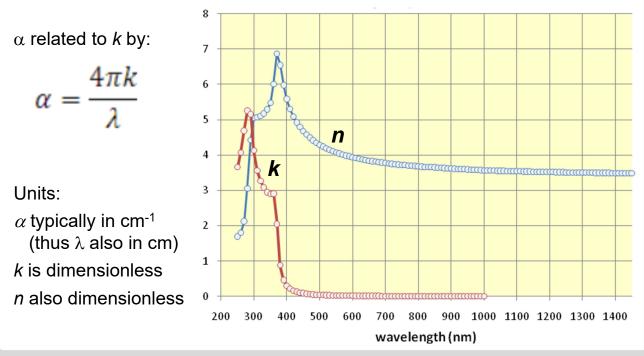


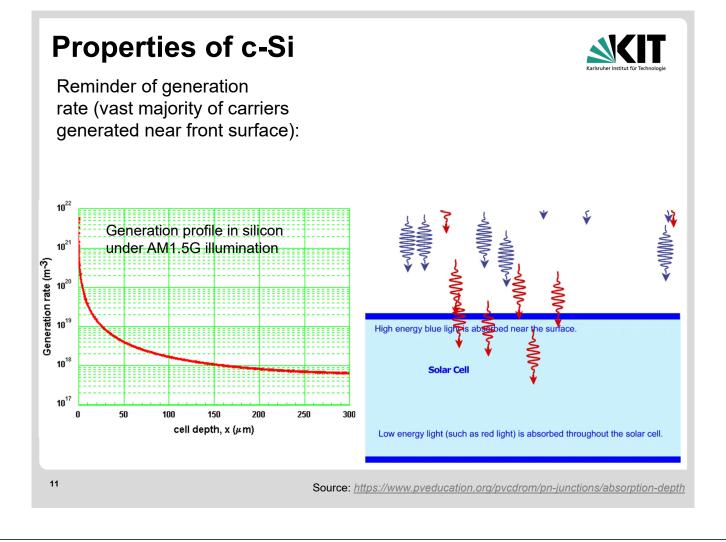
Source: https://www.pveducation.org/pvcdrom/materials/optical-properties-of-silicon

### **Properties of c-Si**



Refractive index (n) and extinction coefficient (k) of silicon







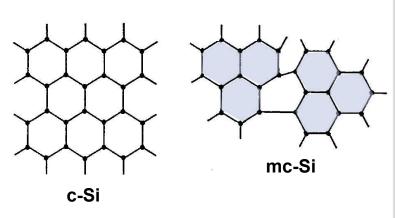
Further impact of indirect nature of c-Si bandgap  $\Rightarrow$  radiative recombination can be neglected  $\Rightarrow$  thus Auger recombination and Shockley–Read–Hall (SRH) recombination dominate

Monocrystalline silicon (a.k.a. single-crystalline silicon)  $\Rightarrow$  crystalline solid in where crystal lattice is continuous and unbroken

Multicrystalline (mc-Si – a.k.a. polycrystalline silicon)

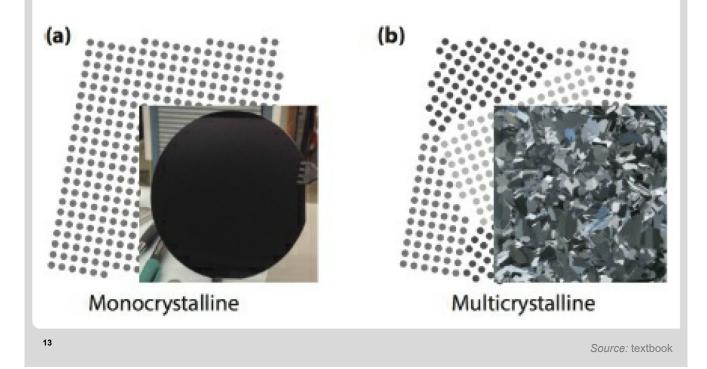
⇒ material consists of many small crystalline grains with random orientations. Between each grain are "grain boundaries"

Results in shorter charge carrier lifetime (i.e shorter *L*) as SRH recombination rate increased (related to  $e^-$  trapped at defect states)





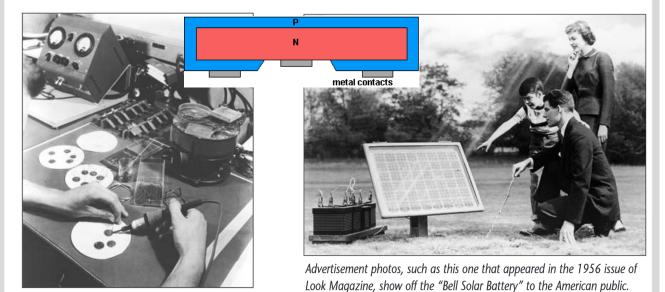
With mc-Si, the differently-oriented grains (crystals) are relatively large ( $mm^2 - cm^2$ ) and clearly visible



#### Silicon – Long History



Forefather of today's Si solar cell date to 1954 by researchers at Bell Laboratories (USA). Cells had a <u>diffused junction</u> and both *n*- and *p*-type contacts on the rear  $\Rightarrow \eta = 6\%$  (15x that of earlier devices). First application for space  $\Rightarrow$  remained major market until early 1970's



Sources: <u>http://www.pveducation.org/pvcdrom/manufacturing/early-silicon-solar-cells</u> <u>http://www.nrel.gov/education/pdfs/educational\_resources/high\_school/solar\_cell\_history.pdf</u>

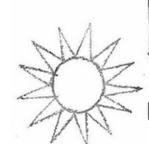
#### Silicon – Long History



all in

#### The Bell Solar Battery.

silicon wafers turns sunshine into 50 watts of electricity. The battery's 6% efficiency approaches that of gasoline and steam engines and will be increased. Theoretically the battery will never wear out. It is still in the early experimental stage.



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Source: http://www.radiomuseum.org/forumdata/users/6435/Cxt/07\_cell.jpg

#### **Refining Silicon**

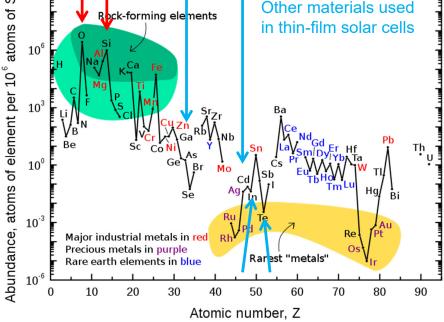


Silicon dioxide  $(SiO_2) \Rightarrow$  most abundant mineral in earth's crust  $\Rightarrow$  used to manufacture pure silicon in two stages

 $10^{\circ}$ 

- 1. Oxygen is removed to produce to produce metallurgical grade silicon
- 2. Further refined to produce <u>electronic</u> <u>grade silicon</u>

An intermediate grade with impurity levels between 1) and 2) above is often termed <u>solar grade silicon</u>



#### **Metallurgical Grade Silicon**



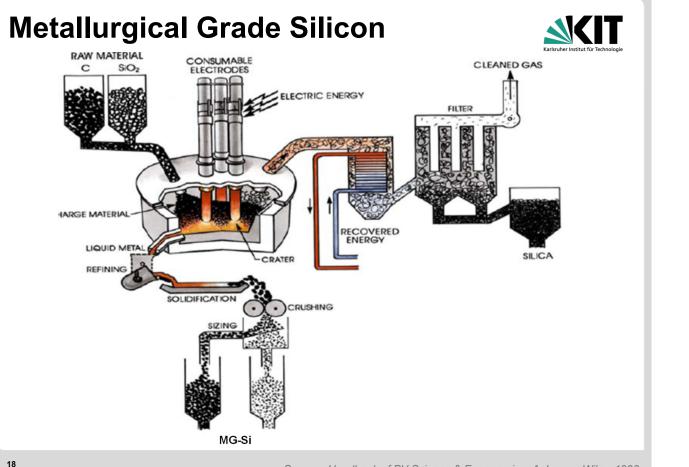
Silica (SiO<sub>2</sub>) occurs naturally as quartz.

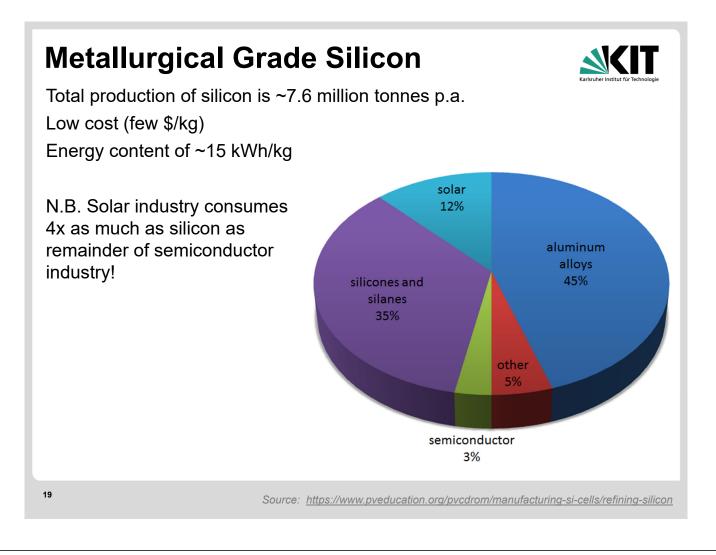
High purity quartz rock is most common raw material for making electronic grade Si, but could also use beach sand. Ideally, silica has low concentrations of Fe, Al and other metals.

Silica is reduced ( $O_2$  removed) via reaction with carbon (coal, charcoal) and heating to 1500-2000 °C in an electric furnace

 $SiO_2 + C \rightarrow Si + CO_2$ 

Result is metallurgical grade silicon (MG-Si)  $\Rightarrow$  98% pure and used extensively in the metallurgical industry (e.g. ~1% Si used for making some Al alloys)



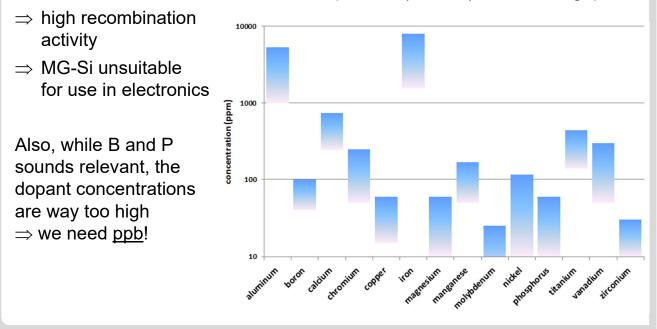


### **Metallurgical Grade Silicon**



2% impurities are mainly carbon, alkali-earth and transition metals and hundreds of ppm of B and P

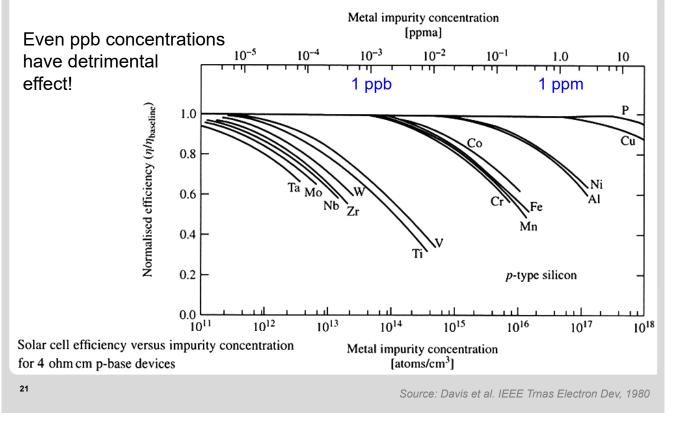
Transition metals in silicon result in deep levels (defects) within bandgap



### **Metallurgical Grade Silicon**



Research in '80s determining effect of impurities on solar cell efficiency



#### **Electronic Grade Silicon**



Thus, MG-Si needs to be further refined for semiconductor applications

Powdered MG-Si reacted with hydrochloric acid (HCl) at  $300^{\circ}$ C in a fluidized bed reactor to form trichlorosilane (TCS, SiHCl<sub>3</sub>)

Si + 3HCl  $\rightarrow$  SiHCl<sub>3</sub> + H<sub>2</sub>

Why? Impurities such as Fe, AI, and B react to form halides (e.g.  $\text{FeCl}_3$ , AICl<sub>3</sub>,...) <u>and</u> SiHCl<sub>3</sub> has low boiling point of 32°C (c.f. 180-300 °C for FeCl<sub>3</sub>, AICl<sub>3</sub>)

 $\Rightarrow$  distillation used to purify and separate SiHCl<sub>3</sub> from impurity halides  $\Rightarrow$  now has < 1 ppb of electrically active impurities

Finally, pure SiHCl<sub>3</sub> is reacted with hydrogen at  $1100^{\circ}$ C for  $\sim 200 - 300$  hours to produce a very pure silicon

 $SiHCl_3 + H_2 \rightarrow Si + 3 HCl$ 

#### **Electronic Grade Silicon (EG-Si)**



Reaction of SiHCl<sub>3</sub> + H<sub>2</sub> takes place inside large vacuum chambers  $\Rightarrow$  Si deposited onto thin polysilicon rods to produce high-purity polysilicon (~Ø20cm)  $\Rightarrow$  "Siemens process" (1960's) Rods of EG-Si then broken  $\Rightarrow$  form

feedstock for crystallisation process Production requires a lot of energy



External (Poly) envelope silicon rods Internal wall - Cooling Electrical contact to resistive Reactor Reactor outlet inlet heating SiHCl<sub>3</sub> SiCl<sub>4</sub>  $H_2$  $(H_2)$ (SiHCl<sub>3</sub>) (SiH<sub>2</sub>Cl<sub>3</sub>) HCl

Source: Handbook of PV Science and Engeneering, A. Luque, Wiley, 1998

#### Single Crystal Silicon

Once we have EG-Si, the Czochralski (Cz) process is most common way to produce single crystal ingots

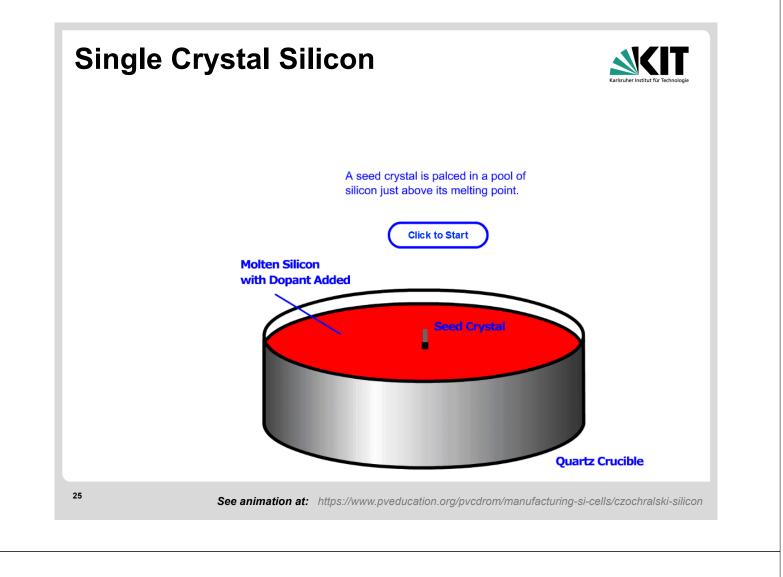
The use of quartz crucibles (see next slide) in manufacture of Cz Si results in

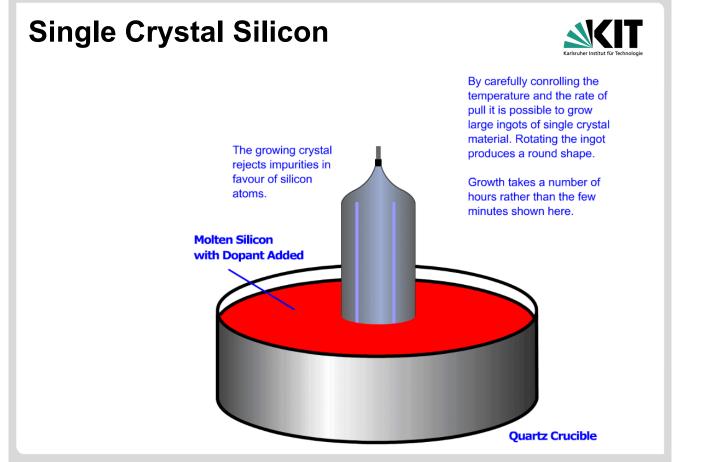
- $\Rightarrow$  incorporation of ppm (10<sup>18</sup> cm<sup>-3</sup>) of O into Si ingot
- $\Rightarrow$  creation of B-O defect that can degrade *L* over time (does not happen in *n*-type ingots fabricated with phosphorus)

Energy content of Cz c-Si ~210 kWh per kg of EG-Si

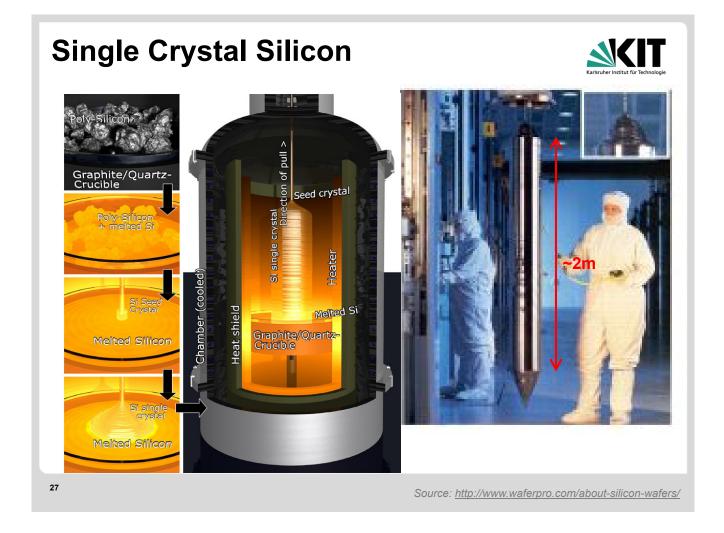


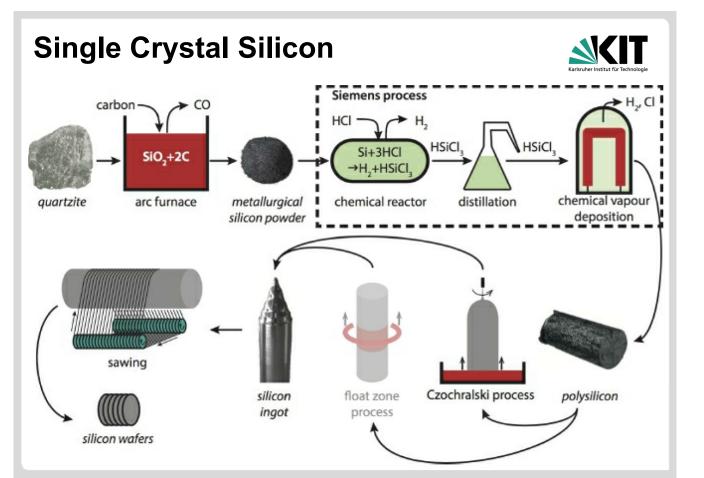






Source: https://www.pveducation.org/pvcdrom/manufacturing-si-cells/czochralski-silicon





#### **Multi-Crystalline Silicon**



Can instead produce mc-Si  $\Rightarrow$  ingots are grown in a large square ceramic crucible:

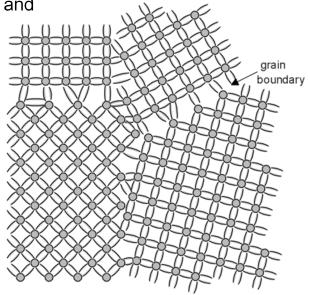
**⊠** simpler,

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- Iess energy intensive (8-15 kWh/kg), and
- 🗹 cheaper, but...
- Image: Image: Second Second

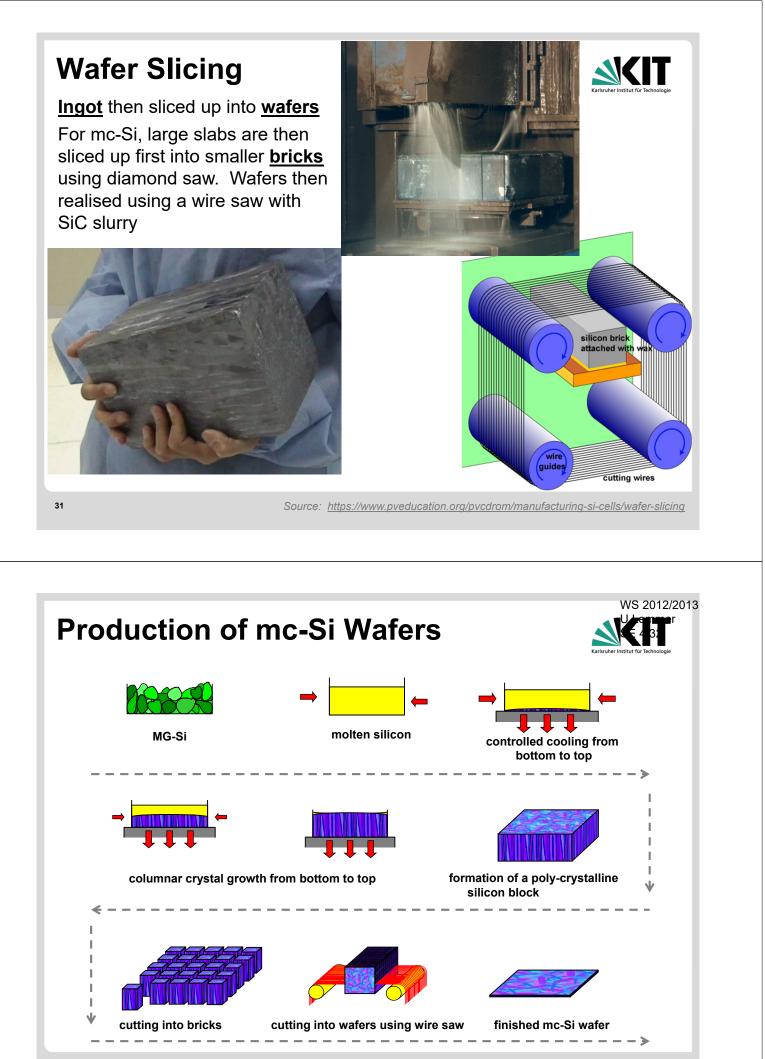
Grain boundaries introduce

- high localised regions of recombination due to introduction of extra defect energy levels into bandgap ⇒ reduces L
- Barriers to flow of carriers and providing shunting paths for current flow across *p-n* junction

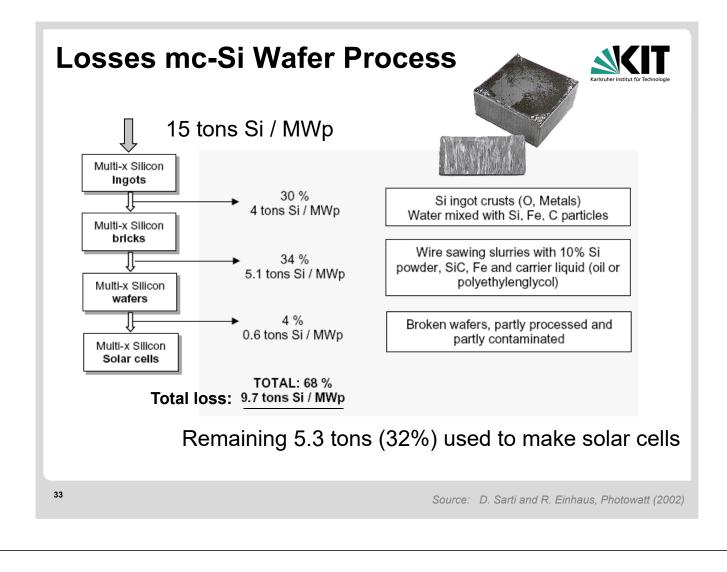


Source: https://www.pveducation.org/pvcdrom/manufacturing-si-cells/multi-crystalline-silicon





Source: Gerhards, Dissertation, Konstanz 2002, U.Kindereit, Studienarbeit, Berlin 2004)



#### **Solid State Diffusion**



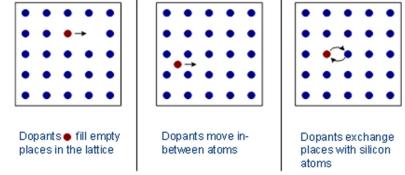
Solid state diffusion: net transport of atoms from a region of higher concentration to one of lower concentration by random molecular motion

 $\Rightarrow$  results in a gradual mixing of materials

e.g. drop of ink in glass of water is evenly distributed after a certain amount of time



In Si crystal, there is a solid lattice of atoms through which the dopant atom has to move. This can be done in different ways:



In Si solar cells, typically start with a uniformly doped *p*-type wafer (the "base") – the *n*-type "emitter" layer is formed via phosphorus doping

#### **Solid State Diffusion**



Reminder – diffusion process follows Fick's law:

$$j = -D\frac{\partial N}{\partial x}$$

where

j =flux density (atoms/cm<sup>2</sup>), D =diffusion coefficient (cm<sup>2</sup>/s) at a given temperature, T N =concentration volume (atoms/cm) x =distance (cm)

Typically, the diffusion of atoms into Si wafer is a 2-step process:

- wafer first placed in a furnace with <u>unlimited source</u> (e.g. full of phosphorus gas)
- 2) then turning off the dopant source (<u>limited source</u>) and driving the phosphorus atoms further into the wafer

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#### **Solid State Diffusion**



1) <u>Diffusion from an unlimited source</u>: produces a shallow junction with a <u>very high surface concentration</u> of P atoms

Best described by complementary error function (erfc)

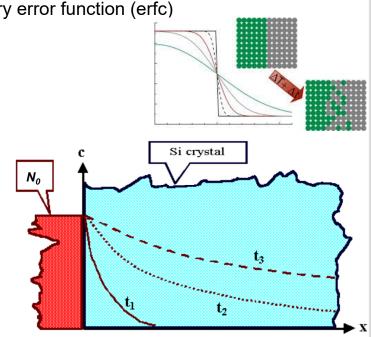
$$N(x,t) = N_0 erfc \frac{x}{2\sqrt{Dt}}$$

where

 $N_0$  = impurity concentration at surface (atoms cm<sup>-3</sup>)

$$t = time (sec)$$

Often called a "pre-deposition" step



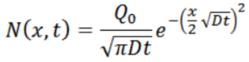
#### **Solid State Diffusion**



2) Diffusion from a Limited Source: consists of two-step process

- i. a short pre-deposition as outlined in 1) above, followed by
- ii. a longer <u>drive-in</u> at a higher temperature (with dopant source removed) to provide a deeper and more lightly-doped emitter

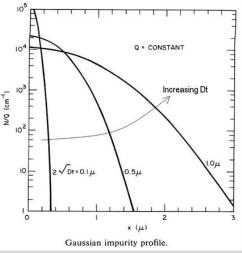
The drive-in is usually at a higher temperature  $\Rightarrow$  now the final dopant profile is described by a Gaussian:



where

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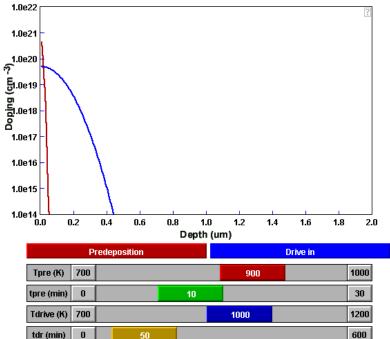
 $Q_0$  = is atoms introduced in the pre-deposition (atoms cm<sup>-2</sup>)

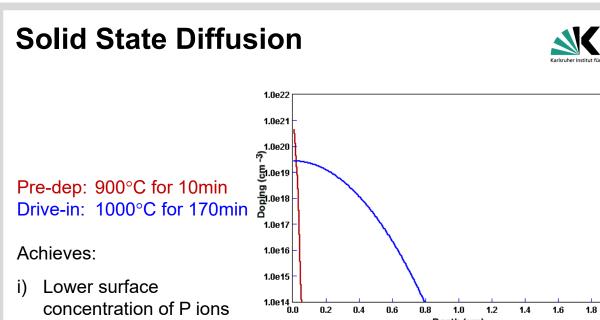


#### **Solid State Diffusion**

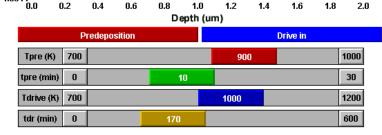
Diffusion of an n-type dopant, phosphorus (P), to create a *pn* junction in a p-type (boron, B) base

Pre-dep: 900°C for 10min Drive-in: 1000°C for 50min





ii) Deeper junction – further away from front surface

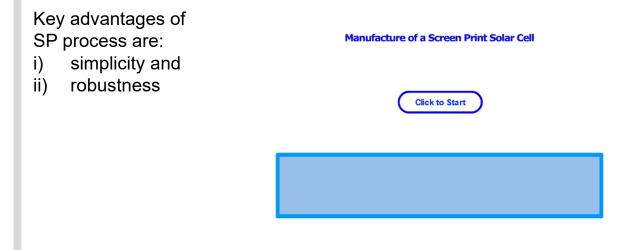


Source: https://www.pveducation.org/pvcdrom/manufacturing-si-cells/solid-state-diffusion

#### **Screen Printed Solar Cells**



Screen-printed (SP) solar cells first developed in 1970's  $\Rightarrow$  remains most mature solar cell fabrication technology  $\Rightarrow$  Still in production today (although higher efficiency devices becoming more common in production in last 2-3 years)

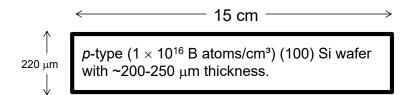




Fabrication sequence:

1. <u>Sawing</u>

of monocrystalline or mc-Si ingots to produce wafers



#### 2. Etching

to remove saw damage (10-20µm from either side of wafer etched off)

Etching away the saw damage

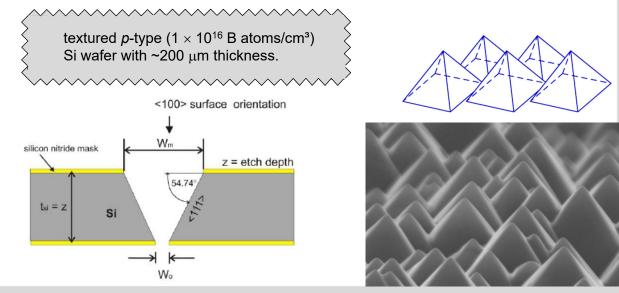
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# **Screen Printed Solar Cells**

Karlsruher Institut für Technologie

Fabrication sequence:

<u>Texturing</u> (only for monocrystalline Si wafers)
 <100> oriented Si wafers are textured ⇒ results in exposing <111> crystal planes using potassium hydroxide (KOH) or sodium hydroxide (NaOH) based anisotropic etch ⇒ 1-10µm high pyramids



Source: <u>www.pveducation.org/pvcdrom/light-trapping</u> Abidin *et al.*, *Jurnal Teknologi* 74. (2015) 10



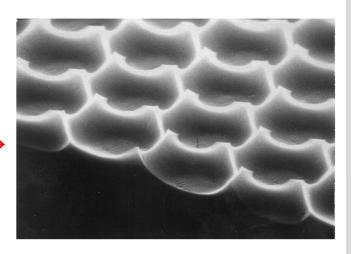
Surface Texturing to Reduce Reflection:

While monocrystalline Si wafers are easily textured using alkaline etch to from pyramids and reduce reflection, same process is only marginally effective on the <u>randomly orientated</u> grains of mc-Si

Various schemes have been proposed to texture mc-Si material:

- mechanical texturing of wafer surface with dicing saws or lasers
- plasma etching
- isotropic chemical etching in combination with a photolithographic mask ——

But, standard practice in industry is to still perform alkaline etching – even though not very beneficial (high throughput, low cost)



Source: https://www.pveducation.org/pvcdrom/design-of-silicon-cells/surface-texturing

#### **Screen Printed Solar Cells**

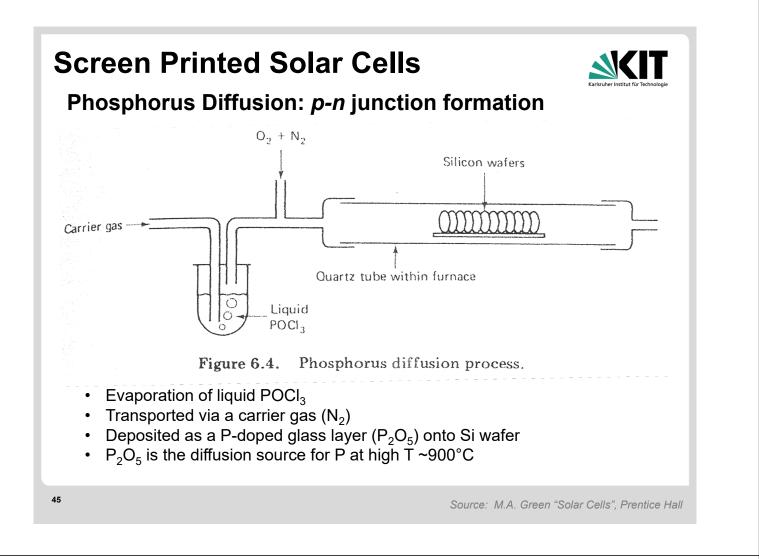
Fabrication sequence:

4. Emitter diffusion

phosphorus diffusion required to form *n*-type emitter on a *p*-type (boron-doped) substrate. Conducted in tube furnace at ~900°C containing phosphorus trioxychloride (POCl<sub>3</sub>)  $\Rightarrow$  deposits a phosphorus glass (P<sub>2</sub>O<sub>5</sub>) layer on top of Si wafer  $\Rightarrow$  acts as a diffusion source for P atoms

n-type emitter

p-type bulk





#### Phosphorus Diffusion: *p-n* junction formation

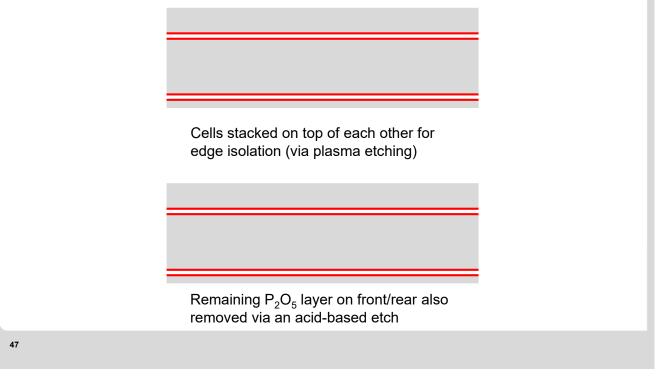






Fabrication sequence:

5. <u>Edge isolation</u> plasma etching used to remove unwanted junction from edge of wafers



### **Screen Printed Solar Cells**



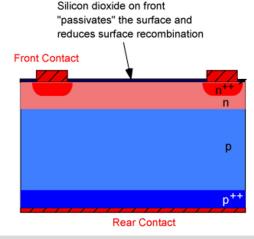
- 6. <u>Passivation and antireflection coating</u> (ARC) the most common ARC material is silicon nitride (a-SiN<sub>x</sub>:H)
  - refractive index  $n \sim 2.2$
  - not only chosen for its optimal refractive index (e.g. in that regard TiO<sub>2</sub> is also good)
  - but also because a-SiN<sub>x</sub>:H affords some <u>passivation</u> of surface and bulk defects (via hydrogen)

n-type emitter		ARC
	p-type bulk	



High recombination rates at top surface have particularly detrimental impact on  $I_{sc}$  (remember highest generation region of carriers occurs at top surface)

Reducing high front surface recombination is typically accomplished by reducing the number of dangling silicon bonds at the top surface by using <u>surface passivation layer</u>, e.g. thermally grown silicon dioxide (SiO<sub>2</sub>) or hydrogenated silicon nitride (a-SiN:H) layers to passivate the surface and reduce defect states at interface



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Source: <u>http://www.pveducation.org/pvcdrom/design/current-losses-due-to-recombination</u>

# **Screen Printed Solar Cells**

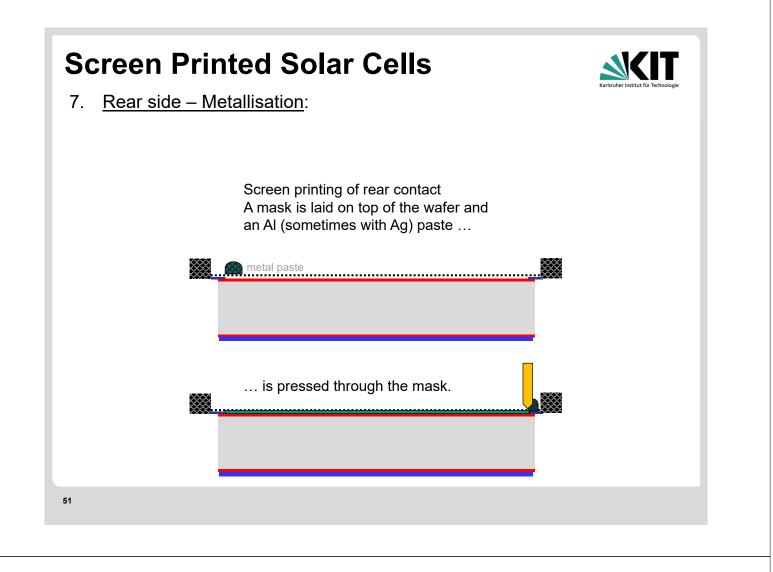
7. Rear side - Metallisation:

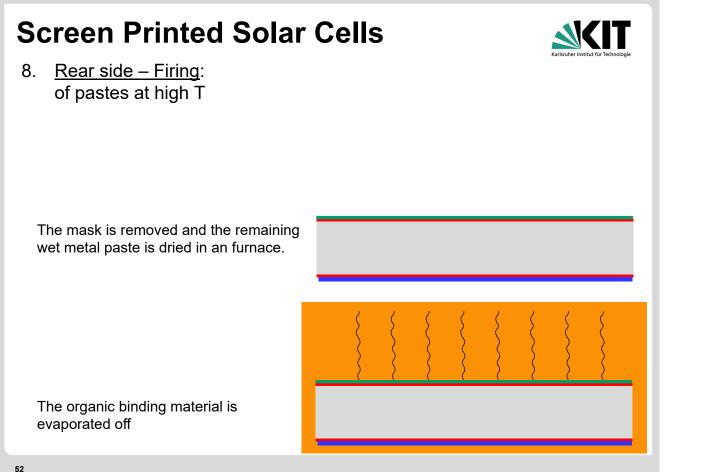
Metal pastes made of three components:

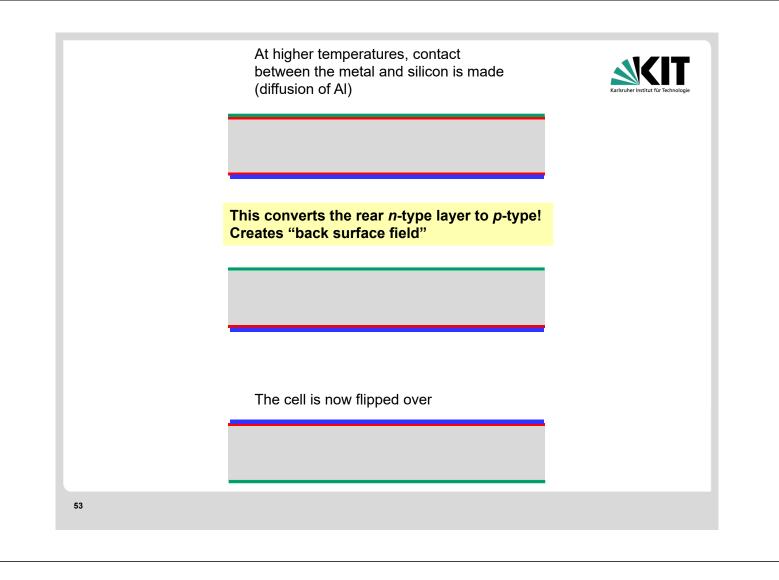
- (a) powdered metal particles  $\Rightarrow$  provides good conductivity
- (b) glass frit  $\Rightarrow$  a binder that helps the silver to adhere to Si substrate and ensure good contact formation
- (c) an organic medium ⇒ disperses the metal powder and glass frit ⇒ e.g. optimised (e.g. viscosity) to be i) printable and ii) obtain a good aspect ratio of finger grids

Disadvantages of screen printing:

- Front contacts can not be finer in width than  $\sim 100 \mu m$
- Particle nature of metal limits conductivity (e.g. to around 1/3 of that of the bulk metal)
- $\Rightarrow$  but screen-printing is still the standard process in industry





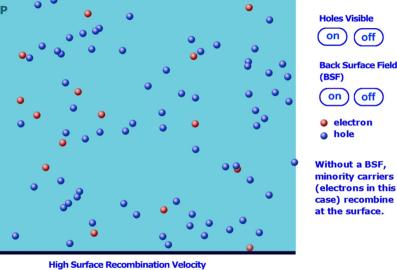




A "back surface field" (BSF) consists of a higher-doped region at rear surface of solar cell. Interface between high- and low-doped region behaves like a *p-n* junction

- $\Rightarrow$  forms electric field at interface
- ⇒ introduces a barrier to minority carrier flow to rear surface by "steering" carriers away from rear surface

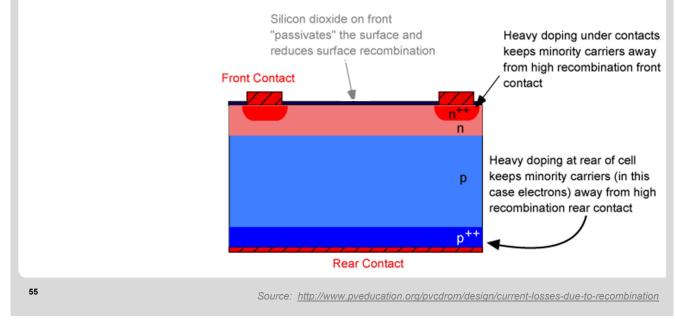
Thus, minority carrier concentration is maintained at higher levels in the bulk of the device  $\Rightarrow$  BSF has net effect of passivating rear surface

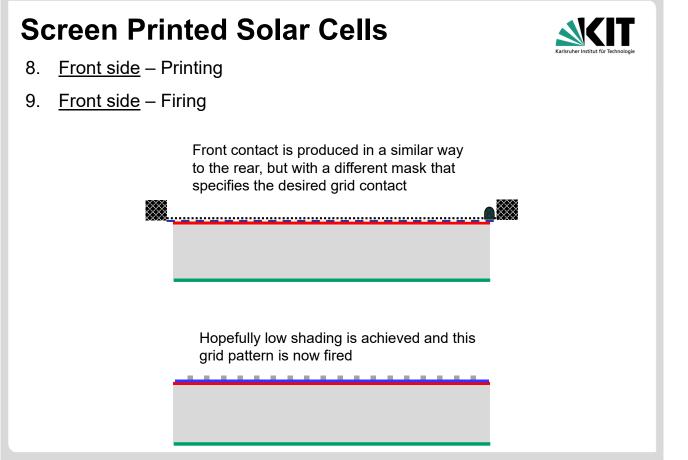


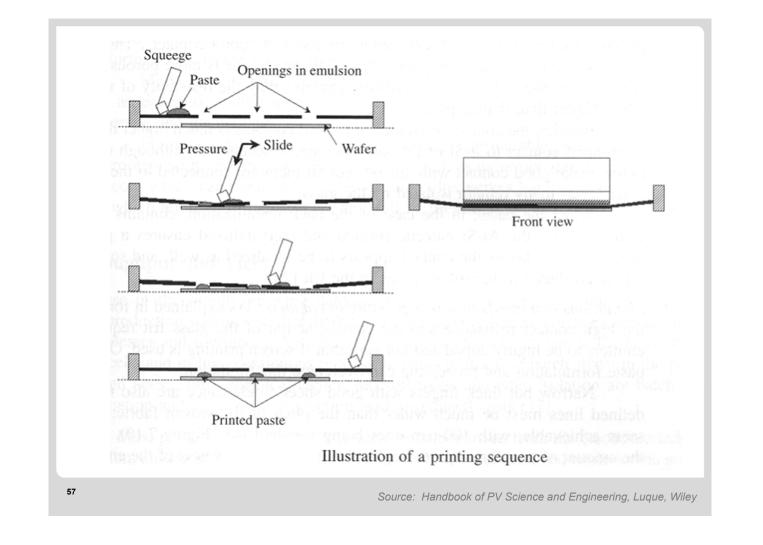


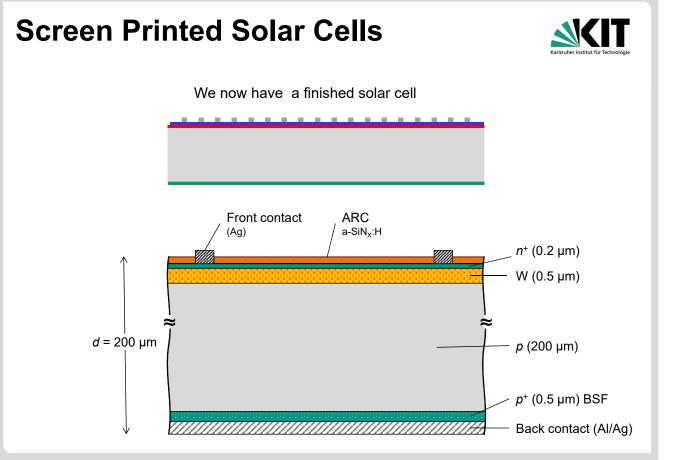
Surface passivation via a dielectric (SiO<sub>2</sub> or a-SiN:H) obviously does not work under an metal contact

Instead, recombination effect minimised by increasing doping (similar approach to BSF)  $\Rightarrow$  high doping severely degrades *L*, but no carrier generation under the contacts

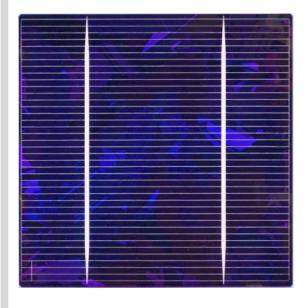


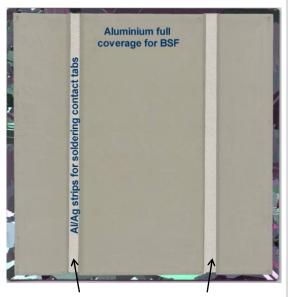












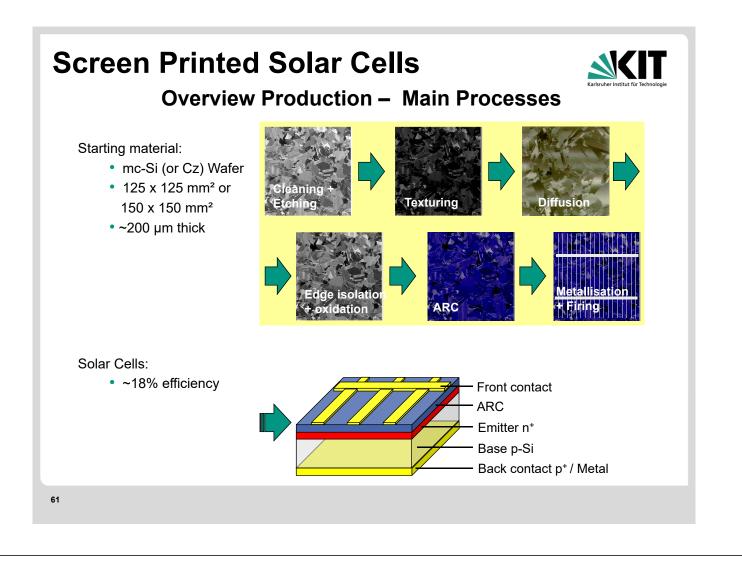
Second Al/Ag SP stripes needed to solder tabbing onto!

#### **Screen Printed Solar Cells**



10. <u>Measurement</u>: under "solar simulator" and sorting into different efficiencies





#### **High-Efficiency c-Si Solar Cells**

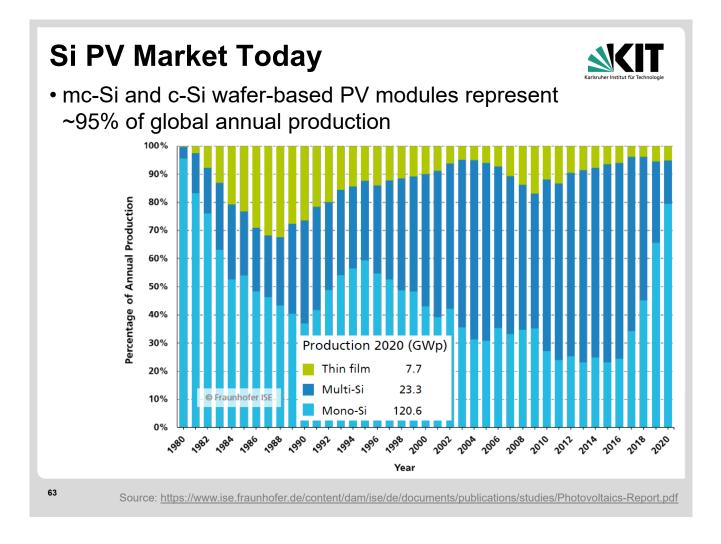


- Several high-efficiency c-Si solar cells exist  $\Rightarrow \eta$  in 22-26% range
- All are based on monocrystalline Si wafers due to lower recombination
- Simple homogeneous (one-step) emitter diffusion for SP solar cells
  ⇒ doping is same beneath metal contacts and in-between fingers
- Trade-off:

a) high surface concentration of P is required below the front metal contact to maintain low contact resistance ( $R_s$ ); vs.

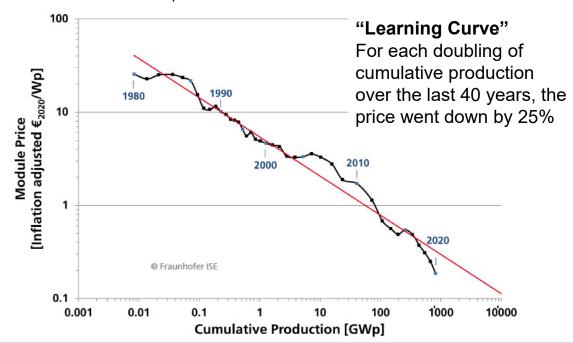
b) <u>but</u> too high a P surface concentration produces a "<u>dead layer</u>"  $\Rightarrow$  which reduces EQE of solar cell in the UV/blue region over entire front surface of solar cell

- Thus, most high efficiency approaches seek to reduce *R*<sub>s</sub> and as well improved the blue response of the solar cell
- Can be realized via "selective emitter" ⇒ a lower doped emitter that then possess much higher doping below the metal contacts ⇒ more complicated as it involves an alignment step



#### **Learning Curve**

• Wafer-based Si PV is constantly decreasing costs and increasing  $\eta$  (\$/W\_p decreasing)



# Summary

- Simple and robust fabrication process for screen-printed PV
- High energy intensity of crystalline silicon... but still cheap?
- mc-Si and c-Si solar cells remain dominant technology
- Si is constantly decreasing costs and increasing  $\boldsymbol{\eta}$
- Today's Si PV technology expected to dominate for at least another decade!
- Hence, wafer-based Si presents all other PV technologies (e.g. thin-film and concentrating PV) with a "moving goal post"



# **Quick Test**



- Why is silicon a good choice as a semiconductor for PV?
- What is the difference between: i) silicon; ii) silica;
  iii) silicone?
- Why can't MG-Si be used to make a working solar cell?
- What are the advantages of mc-Si compared to CZ-Si?
- What trade-offs are there when choosing the dopant profile of the emitter?
- How is the diffusion of P into Si typically realised?
- Why can mc-Si not be effectively etched using the standard alkaline (KOH/NaOH-based) etches for c-Si?
- What technique can we tell whether we have a "dead layer" at the top surface of our solar cell?

